REMARKS

The foregoing amendments, and the following remarks, are deemed fully responsive to the pending office action of August 13, 2004. Claims 1, 3, 4, 8, 9, 12 and 20 are amended without new matter. Claim 2 is cancelled. Claims 1, 3 – 20 remain pending, of which claims 1 and 12 are independent.

A minor amendment is made to paragraph [0007] to clarify that the use of the term "backup" in this paragraph means "return," as opposed to the other use of "backup" meaning a "copy" in the '533 specification.

An amendment is also made to claims 1 and 12 to clarify that the storage of a backup "copy" from the register is made prior to architecting (e.g., writing) data to the register, as per paragraph [0019] of the '533 Application.

Claim Objections

The Examiner objected to claims 3, 4, 9 and 20. Certain amendments are made to these claims to attend to the Examiner's issues. For example, claims 3 and 4 are amended to replace the term "register and" by the term "register". Claim 9 is amended to replace "the step of re-executing' by "a step of re-executing." Claim 20 is amended to replace "further comprising a program counter," by "wherein", and "connection the" by "connection with the."

No new matter is added with these amendments. Reconsideration is requested.

Claim Rejections – 35 U.S.C. § 112

Claim 8 stands rejected under 35 U.S.C. § 112 as failing to set forth the subject matter which applicant(s) regard as their invention. Claim 8 is amended by replacing 'backing up a program counter' with 'resetting a program counter,' as supported for example by paragraph [0006] of the '533 Application: "a program counter is reset to the prior checkpoint, whereinafter processing re-executes program instructions from the last checkpoint."

Reconsideration is requested.

Claim Rejections – 35 U.S.C. § 102

Claims 1, 3-18 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,692,121 issued to Bozso et al. (hereinafter "Bozso").

Respectfully, we disagree. To anticipate a claim, Bozso must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F2.d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Bozso does not teach every element of claims 1, 3-18 and 20.

Rather, Bozso discloses a "method for detecting and correcting errors occurring in mirrored processors." See Bozso, col. 2 lines 24-28. Thus, Bozso specifically requires two processors. In fact, Bozso requires "two processors running identical code in lock-step." See Bozso col. 2, lines 29-31. Claim 1 of the '533 Application concerns the recovery of data errors in a single processor and includes the steps of:

a) storing a copy of data from a register of a register file within a buffer prior to writing new data to the register;
b) periodically checking for data errors within the processor; and
c) restoring the data from the buffer to the register file in the event of data errors.

Checkpoint refers an 'end' of a time period when the processor is checked for errors. In Bozso, "checkpointing or storing" occurs "on a per-instruction basis." See Bozso col. 2 lines 31-34. Thus, Bozso's checkpoint occurs for each instruction executed by both processors. Further, Bozso's checkpoint represents a point when the architectural state of the processor is committed to the recovery unit. Bozso discloses (col. 8, lines 41-44) that "the aggregate Current State array 41a and 41b is transferred to the Checkpoint State array 51a and 51b."

Further, in Bozso "recovery is effected by using the checkpointed state from the architected-state array." See col. 2, lines 51-54. Thus, Bozso's entire architecture of both processors is restored from the architected-state array, whereby the entire architecture of each processor is copied for each instruction and the entire architecture of each processor is restored in the event of error detection.

Accordingly, Bozso does not disclose storing a copy of a register of a register file within a buffer prior to writing new data to the register as required by element a) of claim 1. Note that such a buffer may have "a fraction of the memory capacity of the register file", and may, for example, "include twenty registers as compared to one

hundred twenty eight registers in the register file." See paragraph [0006] of the '533 Application. The architected-stage array of Bozso is simply not equivalent to, and nor does it suggest, claim 1.

Claims 3-12 depend from claim 1 and benefit from like argument. But, in addition, these claims have other features that patentably distinguish over Bozso. For example, claim 3 requires that new data is written to the register after a copy of data in the register is stored within the buffer. Again, Bozso does not teach or suggest storing register data on a register by register basis.

Claim 4 requires that new data is loaded to the register concurrently with the step of loading. Again, Bozso does not teach storing register data on a register by register basis.

Claim 6 requires that the buffer is flushed after checking for, and detecting no, errors. Nowhere does Bozso disclose flushing a buffer.

Claim 8 recites resetting a program counter after detecting errors. Nowhere does Bozso mention resetting a program counter.

Claim 9 recites re-executing a program through the processor at a time associated with the reset program counter. Bozso does not disclose re-executing a program nor resetting a program counter.

Claim 10 recites periodically checking for data errors at sequential time periods defined by a number of processor clock cycles. Contrary to claim 10, Bozso performs "a formal checkpointing or storing ... on a per-instruction basis." See Bozso, col. 2 lines 31-34. The 'checkpointing' period of Bozso is thus defined by each instruction. Clearly, this is different from the claim 10.

Reconsideration of claims 3-11 is requested.

Amended claim 12 recites a processor with register file data recovery, including:

a) an execution unit having a plurality of pipelines for processing program instructions relative to a program counter;
b) a register file, wherein one or more stages of the pipelines loads data to a register of the register file; and
c) a buffer for storing a copy of data within the register and for restoring data to the register file in the event of data errors within the processor.

The pipelines required by element a) of claim 12 are instruction pipelines that have execution units to perform fetch (F), decode (D), execute (E) and write-back (W) operations on instructions within the pipeline. Bozso does not disclose a plurality of pipelines for processing program instructions relative to a program counter. Further, Bozso does not teach or suggest pipeline stages loading data into a register of a register file as required by element b) of claim 12. Bozso therefore cannot anticipate claim 12.

Reconsideration of claim 12 is requested.

Claims 13-18, 20 depend from claim 12 and benefit from like argument; but in addition these claims have other features that patentably distinguish from Bozso. For example, claim 14 recites an extra read port on the register file for reading the data from the register. Bozso does not disclose an additional read port from reading data from the register. Claim 20 requires that the program counter is reset in connection with the buffer restoring data to the register file. Bozso does not disclose a program counter being reset in connection with the buffer restoring data to the register file.

Reconsideration of claims 13-18, 20 is requested.

Claim Rejections – 35 U.S.C. § 103

Claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bozso in view of U.S. 5,568,380 to Brodnax et al. (hereinafter "Brodnax").

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

a) The claimed invention must be considered as a whole;
b) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
c) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
d) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 U.S.P.Q. 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Claim 19 depends from claim 12. Claim 19 recites that the buffer reads data within the register prior to an execution stage for an instruction identifying a write to the register. Brodnax discloses "a fault-tolerant computer system having shadow registers for storing the contents of a primary array into a shadow array at the completion of a stored instruction execution," which "is accomplished on one clock cycle with all registers being shadowed simultaneously." See Brodnax abstract. Neither Bozso nor Brodnax therefore teach or suggest the reading of data from a register of a register file prior to writing to that register. In fact, Brodnax, like Bozso, copies the entire register file at once. In claim 19, on the other hand, data from an individual register is copied to a buffer prior to an execution stage for an instruction identifying a write to the register.

Reconsideration of claim 19 is requested.

For the reasons discussed above, we contend that (a) claims 1, 3-18 and 20 are not anticipated by Bozso and (b) claim 19 is not obvious in view of Bozso and Brodnax. Reconsideration and allowance of claims 1, 3-20 are requested.

Applicants believe no fees are due in connection with this Amendment and Response; however, if any fee is deemed necessary, the Commissioner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

Peter C. Knops, Reg. No. 37,659
LATHROP & GAGE L.C.
2345 Grand Blvd, Suite 2400
Kansas City, Missouri 64108
Telephone: (816) 460-5826
Facsimile: (816) 292-2001